Taskbook - 2021
Communication Systems and Protocols

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Task 1: Data transmission

The Compact Muon Solenoid (CMS) experiment is one of two large general-purpose particle physics detectors built on the Large Hadron Collider (LHC) at CERN in Switzerland and France. On one single day the experiment produces about 20 TB (Terabyte = $1*10^{12}$ bytes) of interesting data. These data has to be transferred to GridKa (Karlsruhe, approx. 450 km distance). The following transport schemes are available:

(i) Transmission over VDSL (50 Mbit/s)
(ii) Transmission over an optical fiber link (110Gbit/s)
(iii) Transport of the data using a hard disk and a car (95 km/h)

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A) Calculate the time required to transfer the data using the different options. Hint: Use 1 Kbit = 1000 bit for the calculation.

In general: time for transmission = $\frac{\text{amount of data}}{\text{data rate}}$

(i) $\frac{\text{amount of data}}{\text{data rate}} = \frac{20{\cdot}10^{12} byte{\cdot}8\frac{bit}{byte}}{50{\cdot}10^{6}\frac{bit}{s}} = 3.2 \cdot 10^{6} s \approx 37\text{days}$

(ii) $\frac{\text{amount of data}}{\text{data rate}} = \frac{20{\cdot}10^{12} byte{\cdot}8\frac{bit}{byte}}{110{\cdot}10^{9}\frac{bit}{s}} = 1454.55s \approx 24.2\text{min}$

(iii) $\frac{\text{distance}}{\text{speed}} = \frac{450km}{95\frac{km}{h}} = 4.7h$

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Task 2: Reflection on wires

A setup consisting of a voltage source with an internal resistance $R_I = 50\Omega$ as sender and a receiver with $R_T = 175\Omega$ is shown in Figure 2. The DC resistance of the line is zero, the characteristic impedance Z_0 is 75Ω.

At the time t= 0 the voltage U_s of the sender changes from $0V$ to $5V$ and is constant afterwards. The run time of a wave on the wire is t_d.

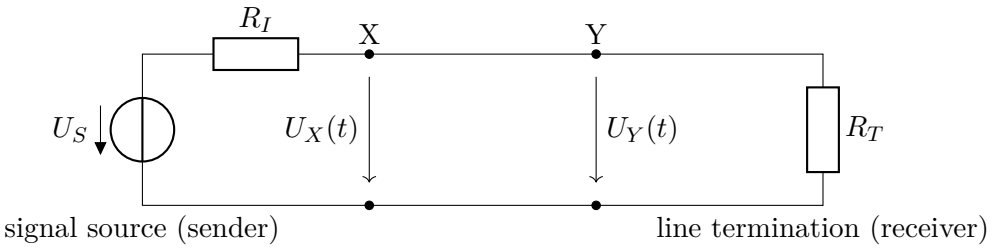

Figure 2.1: Test setup

A) What is the value of the voltage at point X at the time $t = 0$? **1**

At the time of $t = 0$ the wave only „sees“ a series connection of the internal resistance R_I and the wave impedance Zw.

$$U_X(0) = \frac{U_S}{R_I+Z_0} \cdot Z_0 = \frac{5V}{50\Omega+75\Omega} \cdot 75\Omega = 3V$$

B) Which voltage value appears at the points X and Y after an infinite amount of time? **1**

After an infinite amount of time the system is in a steady state, the voltages at points X and Y are identical. When neglecting the DC resistance of the wire a series connection of R_I and R_T remains.

$$U_X(\infty) = U_Y(\infty) = \frac{U_S}{R_I+R_T} \cdot R_T = \frac{5V}{50\Omega+175\Omega} \cdot 175\Omega = 3.\overline{8}V$$

C) Calculate the voltages at the points X and Y at the times $t = 0 \ldots 5t_d$. Neglect all transient events, use ideal rectangular impulses for calculation. **4**

Calculation of the reflection factors

- End of wire: $r_e = \frac{R_T-Z_0}{R_T+Z_0} = \frac{175\Omega-75\Omega}{175\Omega+75\Omega} = 0.4$
- Begin of wire: $r_b = \frac{R_I-Z_0}{R_I+Z_0} = \frac{50\Omega-75\Omega}{50\Omega+75\Omega} = -0.2$

In general:

- Voltage at point X for time t: $U_X(t) = U_Y(t-1)+r_b \cdot [U_Y(t-1)-U_X(t-2)]$
- Voltage at point Y for time t: $U_Y(t) = U_X(t-1)+r_e \cdot [U_X(t-1)-U_Y(t-2)]$

$\Rightarrow U_X(0) = 3V,\ U_Y(1) = 4.2V,\ U_X(2) = 3.96V,\ U_Y(3) = 3.864V,$
$U_X(4) = 3.8832V,\ U_Y(5) = 3.89088V$

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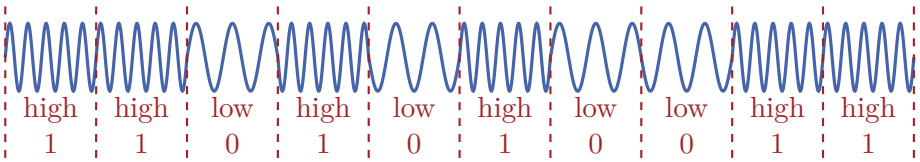
Task 3: Modulation

Give the type of modulation used for the signals as shown in the diagram below. Give also the data that is being transmitted. Assume a constant bit length.

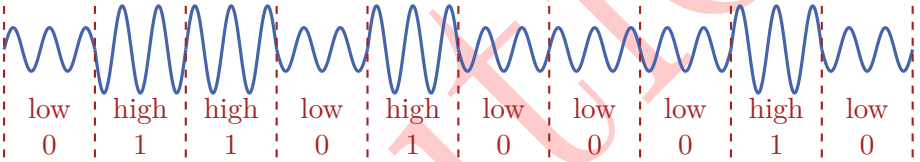
A)



1

1. Determine the changing parameter: Frequency shift keying
2. Determine the points where the signal is changing
3. Read out the signal values
4. Assign signal values to logical values: E.g. high → 1, low → 0

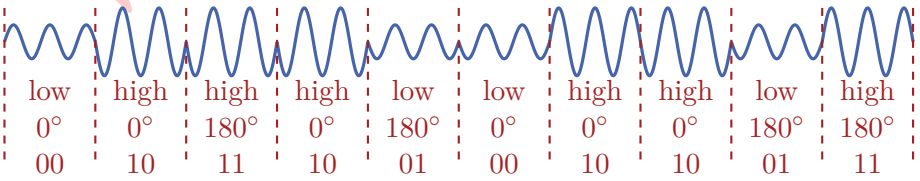
B)



1

1. Determine the changing parameter: Amplitude shift keying
2. Determine the points where the signal is changing
3. Read out the signal values
4. Assign signal values to logical values: E.g. high amplitude → 1, low amplitude → 0

C)



2

1. Determine the changing parameter: Amplitude and Phase → QAM

		Amplitude	
		low	high
Phase	0	00	10
	180	01	11

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Task 4: Line Codes

A) Draw the digital signals for the bit string 101 100 000 011 using each of the NRZ, RZ, NRZI-S, AMI and differential Manchester digital encoding schemes. Use Figure 4.1.

3

1p for each correct line code

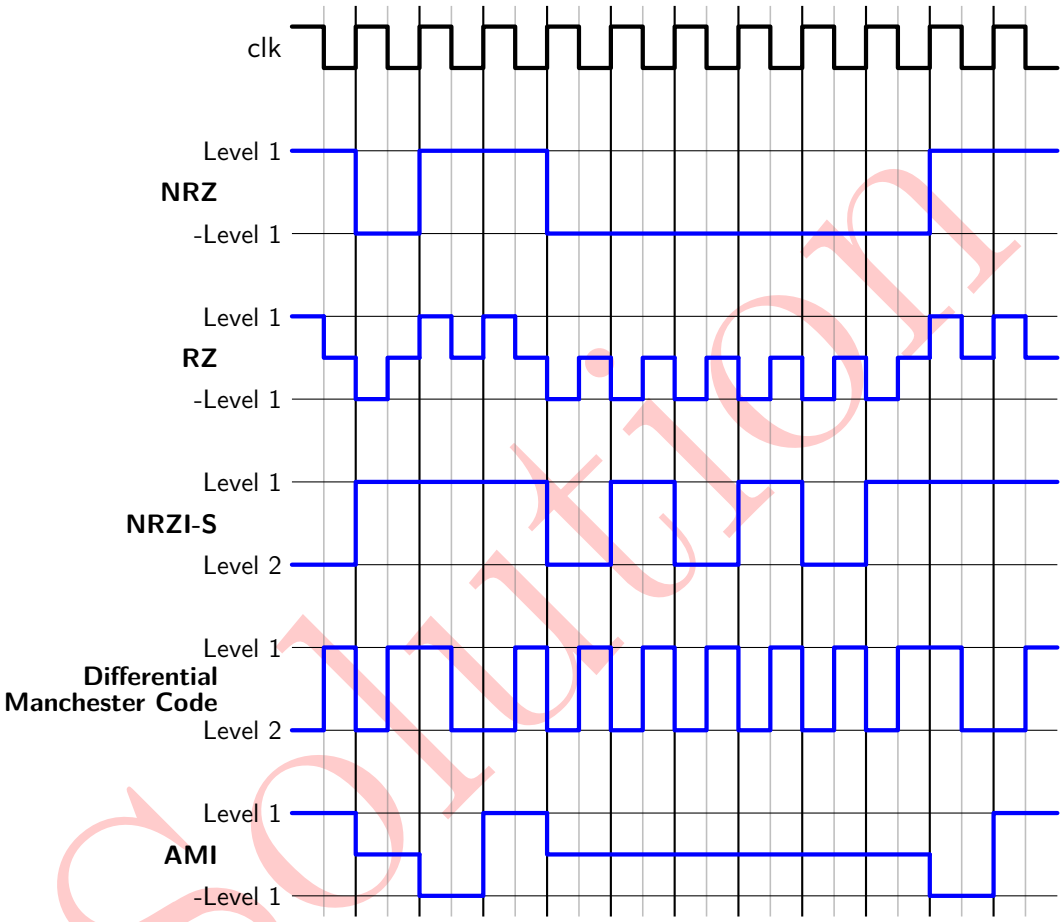

Figure 4.1: Line codes

B) Encode the following bit string using the 4B/5B code:

1

101000001111111000010111

10110 11110 11101 11100 01001 01111

C) What is the longest sequence of "0" if the 4B/5B code is used?

1

The longest sequence contains three "0". For example: 10100 01010

D) What is the longest sequence of "1" if the 4B/5B code is used? **1**

The longest sequence contains eight "1". For example: 01111 11110
On optical fiber, the 4B5B output is NRZI-encoded: A long sequence of "1" serves clock recovery

E) Figure 4.2 shows the signal sequence for a Manchester II coded signal. Determine the associated bit string. **1**

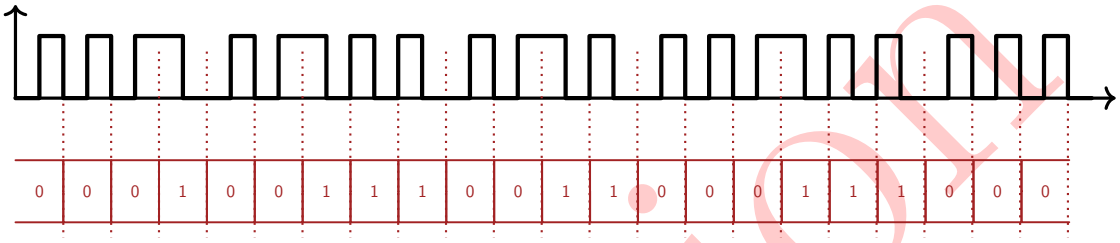

Figure 4.2: Manchester II coded bit string

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Task 5: Physical Basics

Task 5.1: TTL-Logic

A) Insert the logic level (HIGH, LOW) of the output and the state of the transistors (conducts, blocks) into the table 5.1 according to the input configuration x_1 and x_2 at the standard TTL output driver in figure 5.1.

2

-0.5pt per wrong cell, consider consequential errors

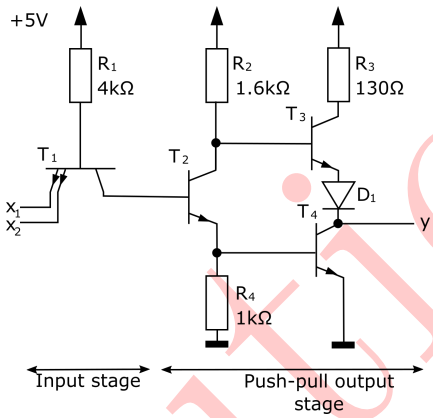


Figure 5.1: standard TTL output driver

x_1	x_2	T_1	T_2	T_3	T_4	y
0	0	conducts	blocks	conducts	blocks	H
0	1	conducts	blocks	conducts	blocks	H
1	0	conducts	blocks	conducts	blocks	H
1	1	blocks	conducts	blocks	conducts	L

Table 5.1: Logic Level

B) List two advantages when using TTL drivers.

1

0.5pt per advantage

High currents are possible;

Valid HIGH and LOW areas are wider at the input due to possible voltage drops on the lines.

C) How would it be possible to overcome the disadvantage of possible short circuits of a TTL driver? Which part of the TTL driver needs to be modified? Modify the Figure 5.2 to get the solution and describe the purpose of te adjustments made.

2

T1 needs an enable input. Additionally a diode in reverse direction is needed between enable and collector of T2.

1pt for correct drawing, 0.5pt for description of enable, 0.5pt for description of diode.

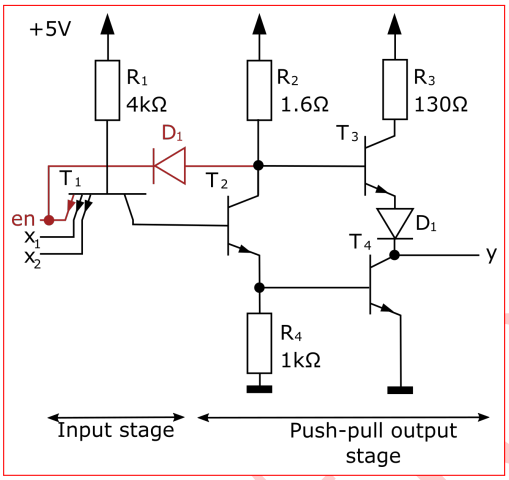


Figure 5.2: TTL driver

Task 5.2: Differential Signals

A) How could differential signal generation be realized?

1

Emitter Coupled Logic (ECL) (with twisted lines)

B) What are the advantages for differential signal transmission? Name two.

1

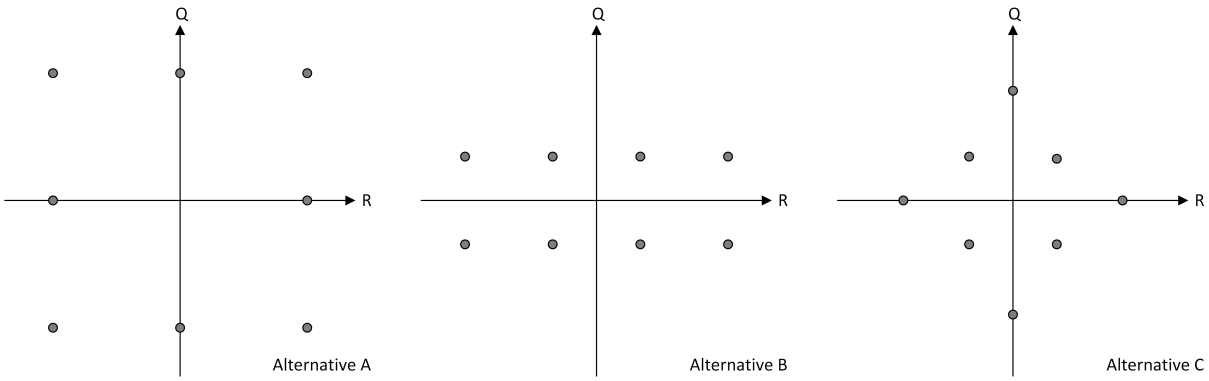
Higher speed since transistors don't go into saturation (ECL)

Inherent compensation of disturbances, noise pulse on both lines and therefore not visible in the differential signal.

0.5pt per correct advantage

Task 5.3: Modulation

Now consider the following constellation diagrams for 8-QAM. All diagrams are drawn with the same scaling of the axes.



A) If you had to realize a communication system using QAM modulation, which alternative would you choose? Give reasons for your decision

2

Alternative A could be chosen because it provides the larges distance between the individual points. Therefore it provides the best resilience against disturbances.

2pt for solution with reasonable explanation. No points for simple answer without explanation. Other solutions can also be correct with proper explanation.

B) Briefly describe PSK modulation and give one advantage.

1

Phase shift keying: Discrete change of the phase of the carrier signal depending on the value to be send. Phase changes can be detected easily thus providing simple and save demodulation

0.5pt for correct description of modulation scheme, 0.5pt for advantage

Task 5.4: Channel capacity, Bandwidth

A digital transmission system with a bandwidth of $B = 1,5 * 10^6 Hz$ has a channel capacity of $C = 5Mbit/s$ (according to Shannon).

A) What is the minimum for the signal to noise ratio (SNR) in dB?

2

$C = B * log_2(1 + S/N)$
$S/N = 2^{(C/B)} - 1 = 2^{(5Mbit/s/1,5*10^6 Hz)} - 1 = 9,079$
$SNR = 10 * lg(2^{(C/B)} - 1) = 9,58dB$

0.5pt for formula, 1.5pt for correct result, -0.5pt if result not in dB

B) Give the definition for the Cut-Off-Frequency:

1

Frequency at which the signal amplitude has dropped by 3db compared to the output value.

Task 5.5: Signal Conversion

A) When converting analog signals into digital signals, what has to be considered in order to be able to achieve an unambiguous reconstruction of the signal (name and formula)? **1**

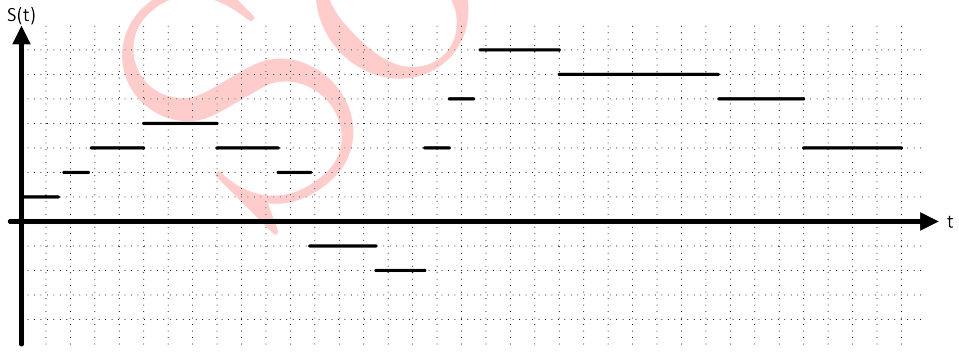
Nyquist-Shannon sampling theorem: $f_{sample} \geq 2 * f_{max}$

B) One can distinguish four different classes of signal. What are the parameters that are changed to form these classes? Give the combination of parameters that are characteristic for each class. **2**

The important parameters are signal value and time. Both can either be continuous or discrete. The four different classes are:

- value-continuous, time-continuous
- value-continuous, time-discrete
- value-discrete, time-continuous
- value-discrete, time-discrete

C) Which signal class does the following signal belong to? Briefly describe where this type of signal can be used. **2**



Signal class name: Time-continuous and value-discrete

Signal usage: Transmission of digital data, e.g. in computer bus systems. As the sampling timepoint is not exactly know before, the signal has to be send continuously. As digital data is to be transported, only discrete values are required.

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Task 6: Wiring

Task 6.1: General Questions

A) What is a symmetric line? Name one disadvantage of symmetric signaling.

1

Transmission of each signal over dedicated signal paths using inverse signal voltages

0.5pt for description
0.5pt for example

One pair of cables are needed for one signal → no reduction is possible, additional overhead for second voltage source and differential receiver.

B) How does the wire length affect the characteristic impedance Z_W in a lossless case?

1

It doesn't affect the characteristic impedance.

C) Name four causes for distortions of real data signals.

1

Noise, bad signal edges, glitches, cross talk, reflections, bad GND, bandwidth issues, (cosmic) Radiation, magnetic/capacitive distortions

0.5p per two correct causes

D) Name the four different possible cases of the reflection factor r and describe shortly their mechanical analogue.

4

- $r = 1$ loose end
- $r = -1$ solid end
- $r = 0$ coupling joint
- $-1 < r < 1$ coupling joint

0.5p for each case
0.5p for aech correct analogue

Task 6.2: Reflection on wires

You have found a transmission link in the basement and want to find out the characteristic impedance. With the setup given in Figure 6.2 you make the measurements that can be seen

in Figure 6.2. The signal source U_S is stuck at an unknown output voltage and has an internal resistance of 33Ω. The termination resistance is $R_T = 200\Omega$. You can assume that the DC resistance is zero. When using numbers from Figure 6.2, only use one decimal place and only use values where the voltage is mostly constant.

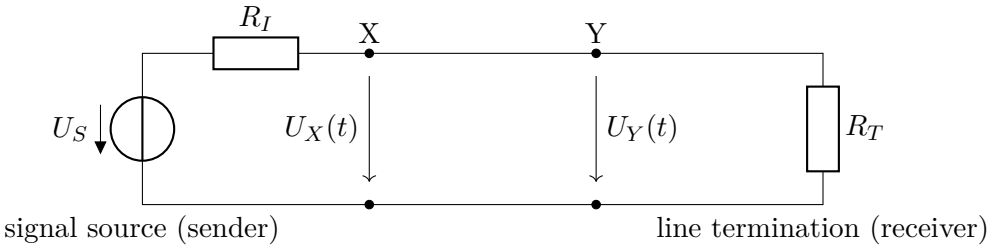

Figure 6.1: Test setup

Figure 6.2: Measurement

A) How would you divide the timeline? Explain and mark at least four points on the timeline **1**

t_d (the propagation time of a wave on the wire) are quite distinct in the figure as the voltages on X and Y change abruptly.

0.5p t_d explained
0.5p two points are marked

B) Without calculation, make a quantitative statement about the reflection factors at the start and at the end. **1**

U_y overshoots U_∞ (and $U_Y(t_1) > U_X(t_0)) \rightarrow r$ at end positive,
value goes down ($U_Y(t_1) > U_X(t_2)) \rightarrow r$ at start is negative

0.5p for estimation
0.5p for reasoning

C) Calculate the characteristic impedance Z_0 and the reflection factors at the start and at the end.

4

1p correct values from figure
1p for Z_0
1p for each reflection factor

At point Y: forward running wave $= 2,7V$
reflected wave $= 1,6V$
$r_e = \frac{1,6V}{2,7V} = 0,59$

At point X: forward running wave $= 1,6V$
reflected wave $= -0,4V$
$r_s = \frac{-0,4V}{+1,6V} = -0,25$

$r_s = \frac{R_I - Z_0}{R_I + Z_0} \Leftrightarrow Z_0 = \frac{R_I - r_s RI}{r_s + 1} = \frac{33\Omega + 8,25\Omega}{0,75} = 55\Omega$

D) Calculate the internal sender voltage U_s

1

0.5p formula
0.5p correct value

$U_X(\infty) = 3.8V$ from Figure

$U_X(\infty) = U_S \frac{R_T}{R_T + R_I} \Leftrightarrow U_S = U_X(\infty) \frac{R_T + R_I}{R_T} = 3.8V \frac{200\Omega + 33\Omega}{200\Omega} = 4,427V$

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Task 7: Data Transmission

Task 7.1: Line Codes

A) Draw the digital signals for the bit string 010 101 111 000 011 using each of the NRZ, Manchester II, and differential Manchester digital encoding schemes. Use figure 7.1.

3

1p for each correct line code

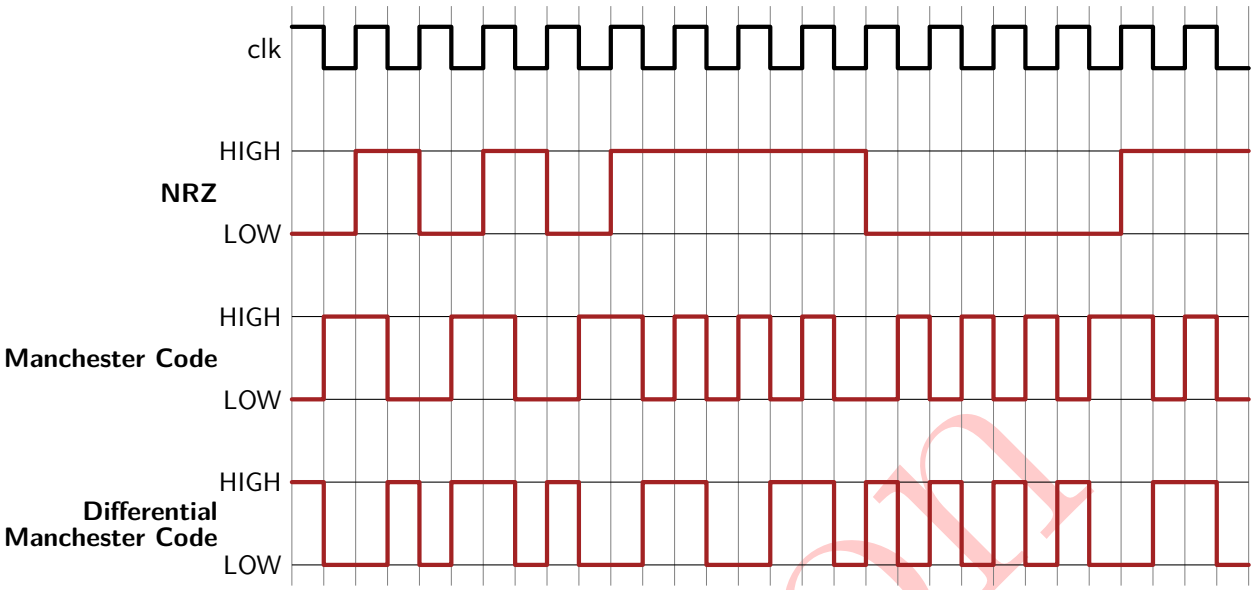


Figure 7.1: Line codes

Task 7.2: CDMA

A) What are the requirements for spreading codes used by CDMA?

1

The spectrum of the spread data function shall look like white noise

Spreading functions have to be orthogonal (orthogonal means that the inner product of two functions equals to 0)

0.5p for each requirement

Sender node	Function
A	$(+1,+1,-1,-1,+1,+1,-1,-1)$
B	$(+1,+1,+1,+1,-1,+1,-1,+1)$
C	$(+1,+1,-1,-1,-1,-1,+1,+1)$

Table 7.1: Functions for sender nodes

B) Table 7.1 shows the functions of several sender nodes. Show that these functions fulfill the requirements and can be used to transmit data using CDMA.

3

requirement: functions have to be orthogonal → inner product of two functions equals to 0)
function node A is orthogonal to function node B:
$(+1,+1,-1,-1,+1,+1,-1,-1)^T \cdot (+1,+1,+1,+1,-1,+1,-1,+1)^T = 0$
function node A is orthogonal to function node C:
$(+1,+1,-1,-1,+1,+1,-1,-1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$
function node B is orthogonal to function node C:
$(+1,+1,+1,+1,-1,+1,-1,+1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$

C) An additional node D should also be able to send data at the same time. Find another function for node D and show that your function is valid.

2

A valid solution: $(+1,-1,+1,-1,+1,+1,+1,+1)$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,-1,-1,+1,+1,-1,-1)^T = 0$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,+1,+1,-1,+1,-1,+1)^T = 0$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$

1p point correct function
1p for prove

Task 7.3: Symbol Stuffing

You want to transmit formatted text but due to limitations of your transmission system you can only use the uppercase letters A-Z and whitespace. However, it should be possible to transmit italic, bold and strike-through text.
To achieve this, the command character "C" is used which denotes the beginning and the end of a command sequence. The commands are then applied to all following characters until the command sequence is repeated. If the character "C" is to be sent as part of the text, it therefore has to be escaped by doubling it at sender site. Available commands are "B" for bold text, "I" for italic text, "L" for lowercase letters and "S" for strike-through text.

A) Format the following text according to these rules: **2**

This task is ~~**stupid**~~ *COOL*

TCLCHIS TASK IS CBSCSTUPIDCBSC CLICCCOOLCIC

1pt for correct starting and ending of commands
0.5pt for correct escaping of "C"
0.5pt for correct sentence

B) What could happen if you did not use commands with an additional separating command word? **1**

Repetitions would be problematic

Task 8: Code Division Multiple Access (CDMA) **7**

A) The transmission scheme "Code Division Multiple Access" uses so called spreading codes to separate different transmissions. One group of functions that can be used for this purpose, are the Walsh functions. The CDMA scheme shall be used for simultaneous transmission of eight different messages. Derive the required Walsh functions. **3**

Function	Code							
0	+1	+1	+1	+1	+1	+1	+1	+1
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	-1	-1	+1	+1	-1	-1	+1
4	+1	+1	+1	+1	-1	-1	-1	-1
5	+1	-1	+1	-1	-1	+1	-1	+1
6	+1	+1	-1	-1	-1	-1	+1	+1
7	+1	-1	-1	+1	-1	+1	+1	-1

B) For the simultaneous transmission of three messages, the Walsh function calculated in this task shall be used. The eight bit given in Table 8.1 shall be encoded each using one of the Walsh functions mentioned above. They are the transmitted simultaneously. The Walsh function is to be inverted when a '0' is to be transmitted and remains unchanged for a '1' to be send. Give the resulting signal on the media. Make use of the given scheme.

2

Node	Data	Signal							
0	"0"	-1	-1	-1	-1	-1	-1	-1	-1
3	"1"	+1	-1	-1	+1	+1	-1	-1	+1
6	"0"	-1	-1	+1	+1	+1	+1	-1	-1
Signal on media		-1	-3	-1	+1	+1	-1	-3	-1

Table 8.1: transmission with CDMA

C) The following Signal has been received from a transmission using the Walsh functions from this task.

2

+2.1 +1.9 +1.4 +2.0 -1.7 +5.3 -2.1 -1.9

As corruptions might happen during transmission, the receiver has a tolerance band for the detection of "1" and "0". All values differing up to ±0.5 from the ideal value will still be accepted as "1" and "0". Calculate the bit value that the receiver will detect for node 1 and node 5.

Node 1

Received	+2.1	+1.9	+1.4	+2.0	-1.7	+5.3	-2.1	-1.9
Node 1	+1	-1	+1	-1	+1	-1	+1	-1
	+2.1	-1.9	+1.4	-2.0	-1.7	-5.3	-2.1	+1.9

-7.6 is in the tolerance band → a "0" has been detected.

Node 5

Received	+2.1	+1.9	+1.4	+2.0	-1.7	+5.3	-2.1	-1.9
Node 5	+1	-1	+1	-1	-1	+1	-1	+1
	+2.1	-1.9	+1.4	-2.0	+1.7	+5.3	+2.1	-1.9

6.8 is not in the tolerance band → error in transmission.

Task 9: Carrier Sense Multiple Access/Collision Detection (CSMA/CD)

2

In this task we have a look at a bus system with arbitration that is derived from CSMA/CD. The following rules apply:

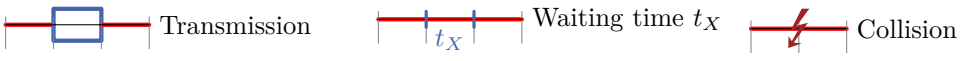
- All nodes want to send as many messages as possible. The length of each message is given in Table 9.1.
- A node is not allowed to send twice in a row. After each successful transmission it has to wait until another node has finished its transmission. The values of the assigned waiting times for each node are given in Table 9.1.
- If a node willing to send detects that the bus is occupied it withdraws and waits for the time specified in Table 9.1 (waiting time) until it will retry to transmit. Any ongoing transmission is not influenced.
- If two or more nodes want to start a transmission on the free bus at the same time there is a collision. All involved nodes withdraw from the bus and wait for the time given in Table 9.1. If a node was already waiting before, its waiting time will be doubled. The waiting time is only reset to the initial value after a successful transmission of the respective node.

Node	Packet length	Waiting time
A	2	1
B	2	2
C	2	3

Table 9.1: Specification of nodes

A) Fill in the signal sequence of the bus nodes, resulting from the specification as given above (use Figure 9.1). Mark waiting times and collisions that occur.

2



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Task 10: Media Access

Task 10.1: CSMA/CD

In this task we have a look at a bus system with arbitration that is derived from CSMA/CD. The following rules apply:

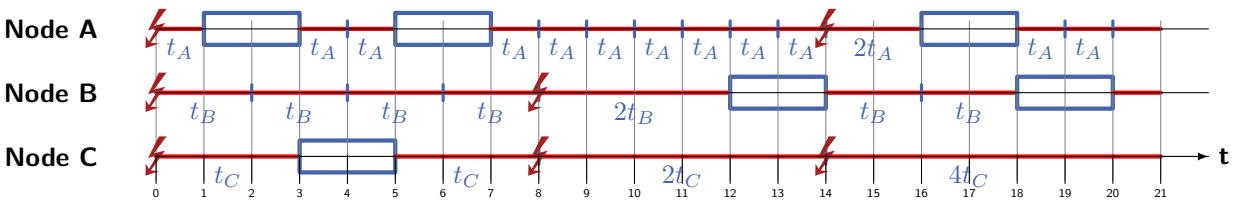


Figure 9.1: Signal sequence

- All nodes want to send as many messages as possible. The length of each message is given in table 10.1
- A node is not allowed to send twice in a row. After each successful transmission it has to wait until another node has finished its transmission. The values of the assigned waiting times for each node are given in table 10.1.
- If a node willing to send detects that the bus is occupied it withdraws and waits for the time specified in table 10.1 (waiting time) until it will retry to transmit. Any ongoing transmission is not influenced.
- If two or more nodes want to start a transmission on the free bus at the same time there is a collision. All involved nodes withdraw from the bus and wait for the time given in table 10.1.

Node	Packet length	Waiting time
A	1	2
B	2	2
C	3	2

Table 10.1: Specification of nodes

A) Fill in the signal sequence of the bus nodes, resulting from the specification as given above (use Figure 10.1). Mark waiting times and collisions that occur. 1

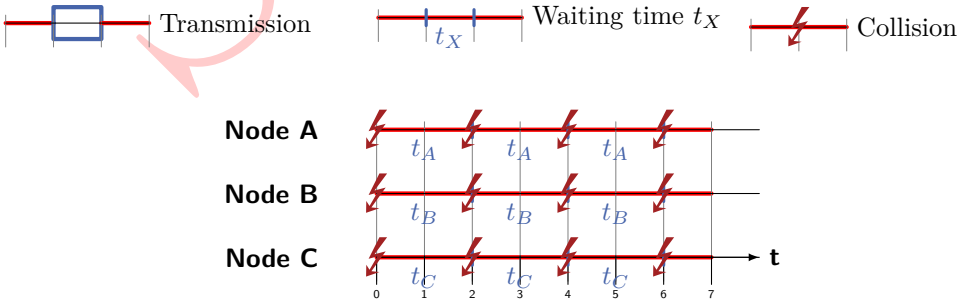


Figure 10.1: Signal sequence

B) Which problem occurs and how could it be solved? 1

Identical waiting time causes many collisions, transmitting is impossible. The waiting time has to be changed so that every node has a different waiting time.

+0.5p for collisions
+0.5p for solution

C) The packet length is unchanged and node C has the highest priority. Modify the waiting times so that all nodes have send data after nine clock cycles (use table 10.2). The waiting times should be as short as possible. Fill in the signal sequence of the bus nodes, resulting from the modified waiting times (use Figure 10.2). Mark waiting times and collisions that occur, label which graph should be evaluated with a cross.

5

+1 P for tc=2
+1 P for tb=3
+1 P for tc=4

Node	Packet length	Waiting time
A	1	4
B	2	3
C	3	2

Table 10.2: Modified waiting time

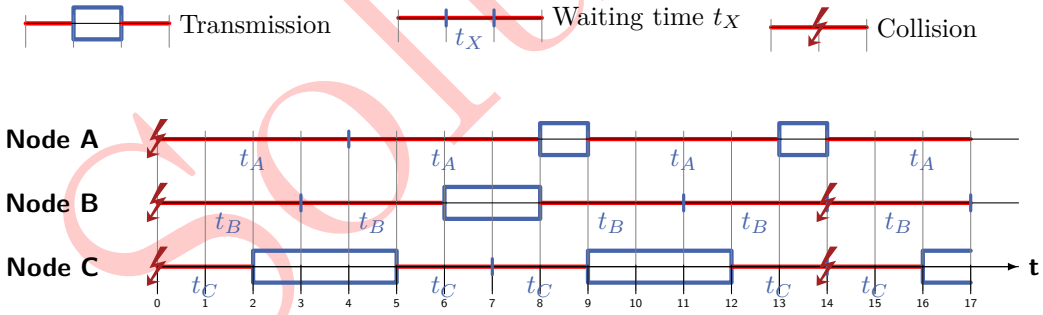


Figure 10.2: Signal sequence

Task 10.2: CSMA/CA

A communication system comprises five communication nodes that use CSMA/CA as arbitration scheme. In order to transmit data a node transmits a dominant start bit (‚0‘) for synchronization purpose. After that a 5 bit message identifier followed and 10 bits of payload data is sent. The message identifiers are unique for each node and all data is sent MSB first. The bus has to cover a maximum distance of $500m$.

A) Name two advantages and two disadvantages of CSMA/CA.

2

Advantages

0.5p for each advantage or disadvantage

- no collisions on the bus
- easy to prioritize because of individual identifiers
- partly real-time capable with additional rules
- efficient use of bandwidth

Disadvantages

- length of the bus and data transmission rate are limited because of simultaneity requirement
- relatively slow (arbitration phase for each message)
- bus can blocked by one node

B) Which requirements have to be fulfilled in order to guaranty a faultless function of the system? What are the implications for the transmission rate?

1

The requirement of simultaneity has to be fulfilled.
The signal propagation time t_s is much smaller compared to the digit length (bit time) t_b:
$\left[t_s = \frac{l}{v}\right] << \left[t_b = \frac{1}{TR}\right]$.

+0.5P for Simultaneity
+0.5P for Transmission rate formula

C) Calculate the maximum payload data rate of this bus. Assume a propagation time of $0.66c$ ($c = 3 \cdot 10^8 \frac{m}{s}$).

2

Transmission rate:
$\left[t_s = \frac{l}{v}\right] << \left[t_b = \frac{1}{TR}\right]$ with $l = 500m$, $v = 0.66 \cdot 3 \cdot 10^8 \frac{m}{s}$

$TR << \frac{v}{l} = \frac{0.66 \cdot 3 \cdot 10^8 \frac{m}{s}}{500m} = 396000 \frac{1}{s}$

Start bit + 5 bit message identifier and 10 bits data:
payload data rate $= \frac{10}{16} \cdot TR = 247500 \frac{1}{s}$

1P for transmission rate
+1P for payload data rate

D) Figure 10.3 shows a timing diagram for the bus system described above. Indicate the identifiers of the given nodes as far as possible (use Table 10.3). Mark undetermined identifiers bits as X!

2

E) Which node is granted exclusive access to the bus?

1

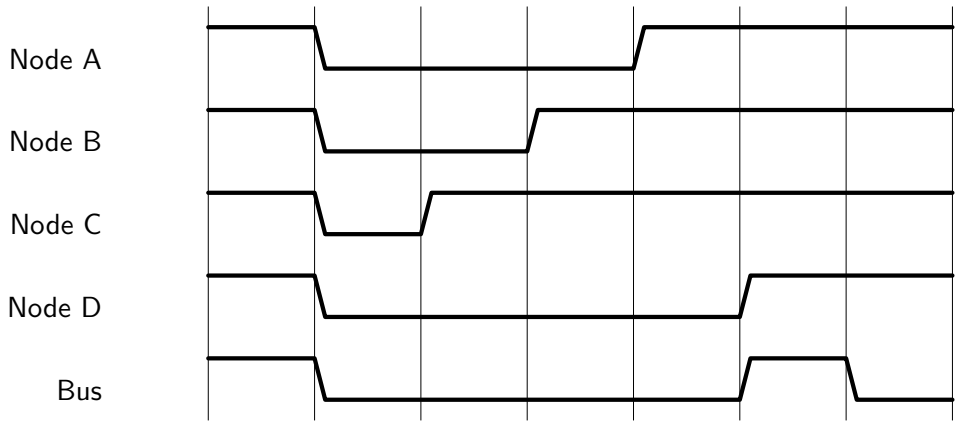


Figure 10.3: Bus Access

Node	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
A	0	0	1	X	X
B	0	1	X	X	X
C	1	X	X	X	X
D	0	0	0	1	1

-0.5pt for each correct line

Table 10.3: Identifiers of the nodes

Node E (five nodes are mentioned in the task) is able to send data.
OR: No one of the four nodes A-D is allowed to send data.

13

Task 11: Spreading Codes

A) Table 11.1 shows the functions of several sender nodes. Show that these functions fulfill the requirements and can be used to transmit data using CDMA. 3

requirement: functions have to be orthogonal → inner product of two functions equals to 0)
function node A is orthogonal to function node B:
$(+1,+1,-1,-1,+1,+1,-1,-1)^T \cdot (+1,+1,+1,+1,-1,+1,-1,+1)^T = 0$
function node A is orthogonal to function node C:
$(+1,+1,-1,-1,+1,+1,-1,-1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$
function node B is orthogonal to function node C:
$(+1,+1,+1,+1,-1,+1,-1,+1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$

Sender node	Function
A	$(+1,+1,-1,-1,+1,+1,-1,-1)$
B	$(+1,+1,+1,+1,-1,+1,-1,+1)$
C	$(+1,+1,-1,-1,-1,-1,+1,+1)$

Table 11.1: Functions for sender nodes

B) An additional node D should also be able to send data at the same time. Find another function for node D and show that your function is valid. 2

A valid solution: $(+1,-1,+1,-1,+1,+1,+1,+1)$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,-1,-1,+1,+1,-1,-1)^T = 0$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,+1,+1,-1,+1,-1,+1)^T = 0$
$(+1,-1,+1,-1,+1,+1,+1,+1)^T \cdot (+1,+1,-1,-1,-1,-1,+1,+1)^T = 0$

1p point correct function
1p for prove

C) Table 11.2 shows the walsh code for a system with four different senders. Only three instead of four senders want to send data. Calculate the resulting signal on the media. 2

Node A	-1	-1	-1	-1
Node B	+1	-1	+1	-1
Node C	+1	+1	-1	-1
signal	+1	-1	-1	-3

Sender node	Function	Data
A	$(+1, +1, +1, +1)$	"0"
B	$(+1, -1, +1, -1)$	"1"
C	$(+1, +1, -1, -1)$	"1"
D	$(+1, -1, -1, +1)$	-

Table 11.2: Walshcode for four sender nodes

D) Calculate the bit value that the receiver will detect for node D. **2**

signal	+1	-1	-1	-3
Node D	+1	-1	-1	+1
	+1	+1	+1	-3

zero is not an accepted value → error in transmission.

E) Assume there is not an analog signal on the media, but a positive and negative value. Calculate the bit value that the receiver will detect for node A and node D. Hint: Think about the tolerance band, when reducing the bandwith of the signal **2**

Node A:

signal	+1	-1	-1	-1
Node D	+1	+1	+1	+1
	+1	-1	-1	-1

$-2 \rightarrow$ A "0" is detected.
Node D:

signal	+1	-1	-1	-1
Node D	+1	-1	-1	+1
	+1	+1	+1	-1

$+2 \rightarrow$ D "1" is detected.

F) Is it useful to send only two different values instead of the analog signal? Justify your answer! **2**

No, the reason is given in the subtask before. The information if a sender sended any data is lost

4

Task 12: Arbitration

2

A) A system using centralized daisy-chaining is shown in figure 12.1. An exemplary arbitration cycle of the system is shown in figure 12.2. Assign the correct signals of figure 12.1 to the signals shown in the diagram below (figure 1.2). Justify your choice of assignment with a few sentences. What node is sending data at which point in time? Complete the diagram (figure 12.2) accordingly.

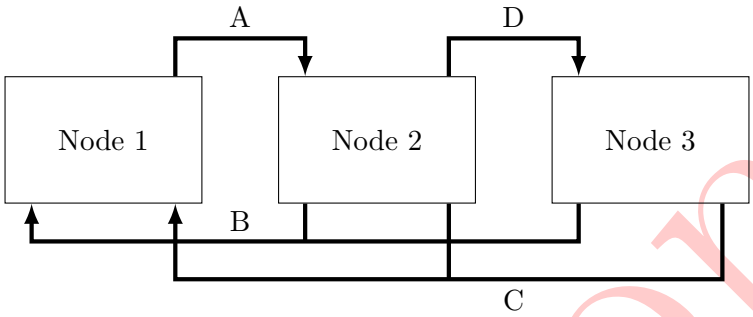


Figure 12.1: Centralized Daisy-chain

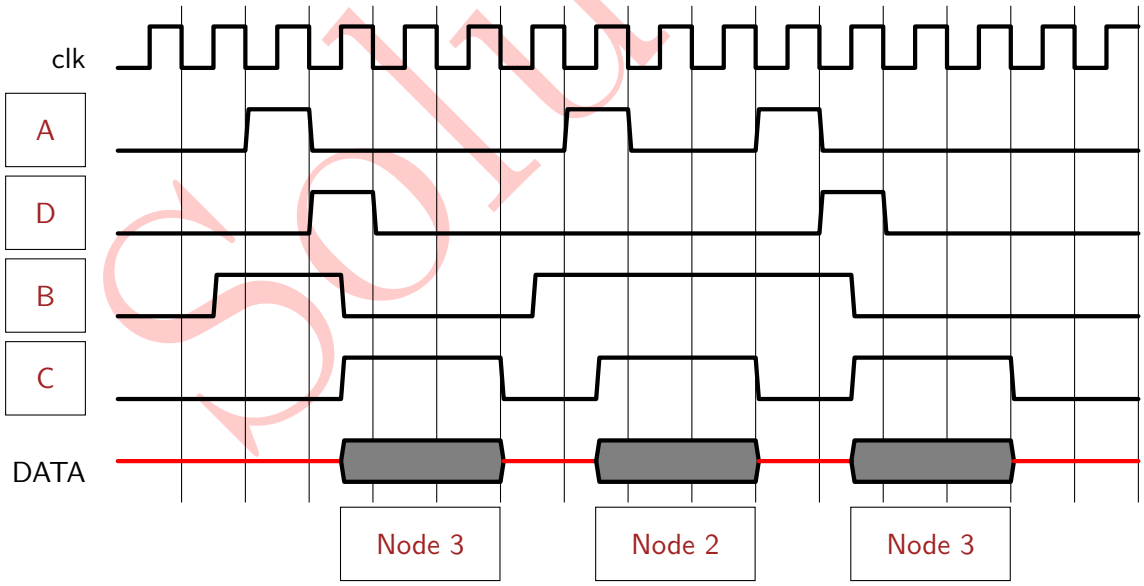


Figure 12.2: Signal flow for Daisy-chain

B) In the decentralized Daisy-chain shown in figure 12.3 a scheduling should be done. The different nodes will set a request at the times given in table 12.1. Only after successful transmission the nodes will remove their request. The sending of the data always needs exactly one time step. This includes token passing and the time needed for the arbitration. Complete Table 12.2 according to the specified arbitration scheme.

2

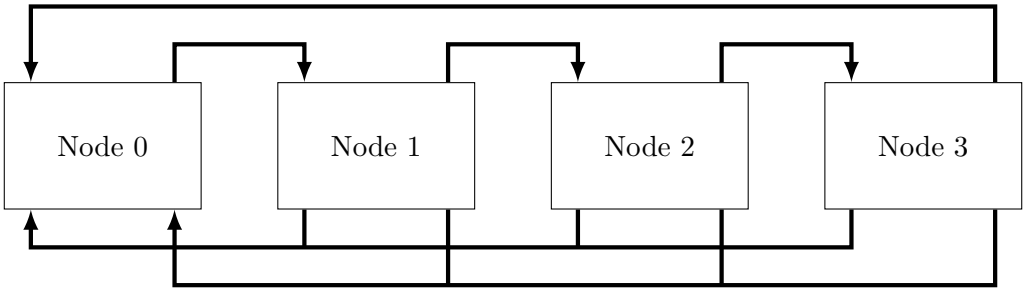


Figure 12.3: Decentralized Daisy-chain

time	Nodes that assert a sending request signal
t_1	Node 2 and Node 3
t_2	Node 1
t_3	Node 0
t_4	Node 0 and Node 1

Table 12.1: Time of sending nodes

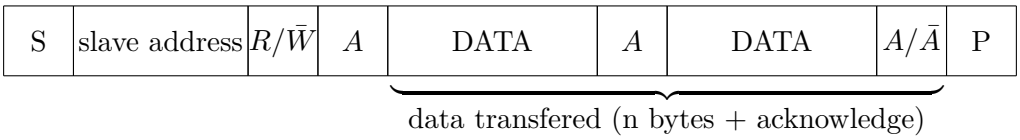
time	Sending Node
t_0	Node 0
t_1	Node 2
t_2	Node 3
t_3	Node 0
t_4	Node 1
t_5	Node 0
t_6	Node 1

Table 12.2: Solution of Daisy-chain scheduling

4

Task 13: I²C-Bus Arbitration

The frame format of I²C-bus is shown in figure 13.1. Three master nodes are simultaneously trying to transmit one byte of data to different slaves over the I²C-bus.



term	descripion
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave
$\bar{A}$	not acknowledge
DATA	8-bit data
P	stop Condition

Figure 13.1: I²C-bus frame format

4

A) The addresses of the slaves and the data to be send to them is shown in the table 13.1. Complete the signal diagram in the figure 13.2.
Hint: A slave always answers with a positive Acknowledge (0). Which node is winning the arbitration?

node	slave address	data
Master 1	0100110	00011010
Master 2	0100101	10100111
Master 3	0100101	00101101

Table 13.1: test

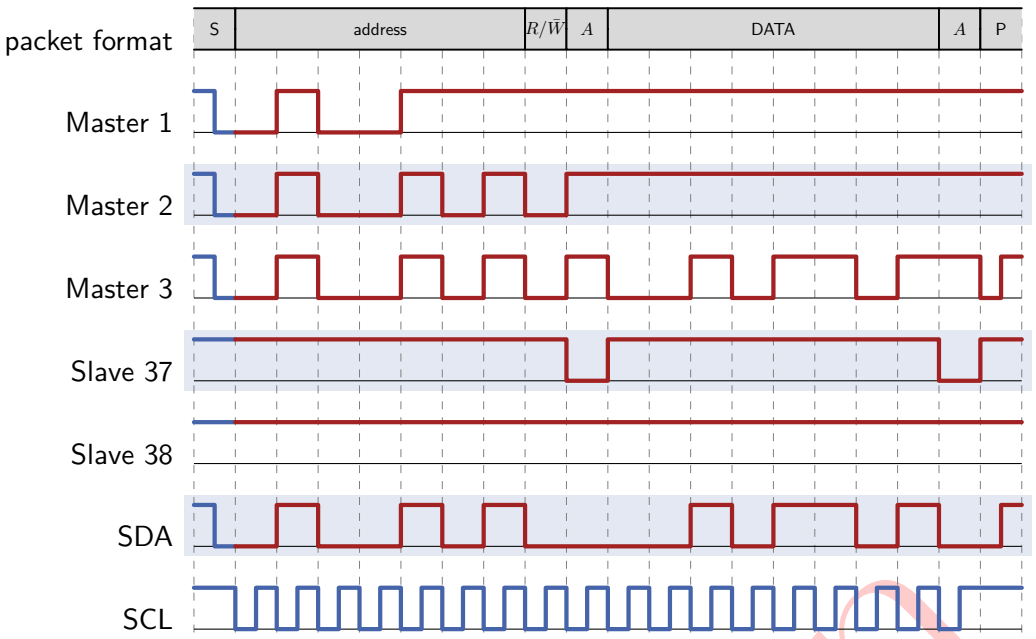


Figure 13.2: Signal sequence

8

Task 14: Cyclic Redundancy Check

Task 14.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial. 1

Polynomial Generator: $1 \cdot x^2 + 0 \cdot x^1 + 1 \cdot x^0 \rightarrow$ Bitstring: 1 0 1

B) What is the length of the checksum that is to be appended to the data stream? 1

Length of the checksum = Order of polynomial generator. here: order $g(x) = 2$

C) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101. 2

```
1 0 0 1 0 1 0 1 0 1 0 0      :      1 0 1
1 0 1
0 0 1 1 0
    1 0 1
    0 1 1 1
      1 0 1
      0 1 0 0
        1 0 1
        0 0 1 1 0
            1 0 1
            0 1 1 1
              1 0 1
              0 1 0 0
                1 0 1
                0 0 1 0  remainder
```

Bit string to be transmitted: 1001010101 10

Task 14.2: Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A) Denote the bit stream as it arrives at the receiving node. **1**

Received bit stream: 100101011001

B) Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used. **2**
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

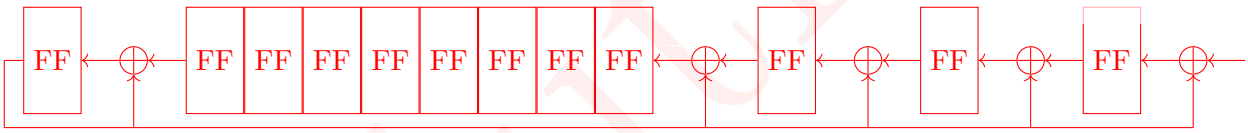
```
1 0 0 1 0 1 0 1 1 0 0 1      :      1 0 1
1 0 1
0 0 1 1 0
    1 0 1
    0 1 1 1
      1 0 1
      0 1 0 0
        1 0 1
        0 0 1 1 1
            1 0 1
            0 1 0 0
              1 0 1
              0 0 1 0 1
                  1 0 1
                  0 0 0  remainder
```

Generator polynomial is too short to detect a burst error of length 4.

Task 14.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$).

1



6

Task 15: I²C-Bus Synchronization

Three I²C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is neglectably small (0 time steps). The individual masters want to establish a clock signal according to the following table 15.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 15.1: clock signals

Assume that Master B is initiating the communication cycle.

A) In general, which functionality does the I²C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node? **1**

The I²C-Bus uses clock synchronization and arbitration (over the complete dataframe, over address and data fields).

B) Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal. **3**

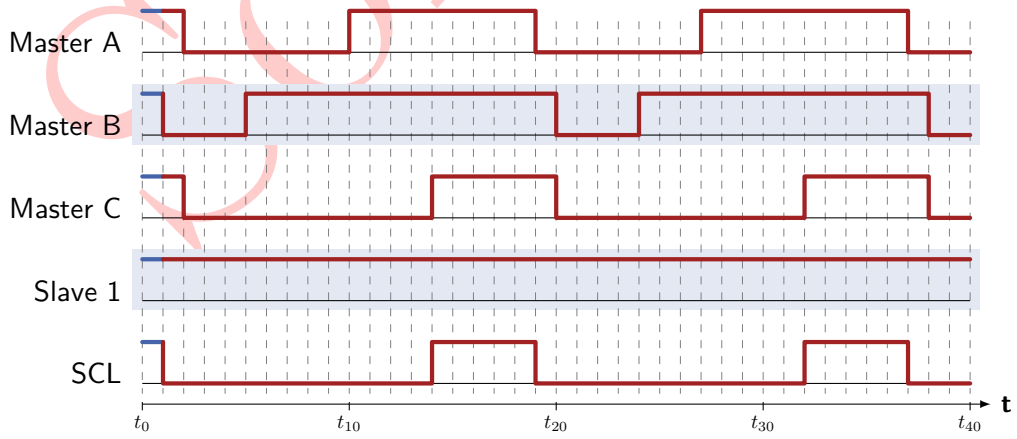


Figure 15.1: Signal sequence

C) In general, which functionality does the I2C bus provide for the case when there is a fast and a slow master node? **2**

The I^2C-Bus uses a kind of handshake mechanism that allows slower nodes to insert wait states if the other node is too fast. The wait state insertion is controlled by the SCL signal. In general, the SCL signal is generated by a wired-AND connection with dominant "0" of the participants CLK signals. A wait state is inserted if the SCL signal remains "LOW" and is initiated by a slower node

6

Task 16: Actuator Sensor Interface (ASI)

In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 16.1.

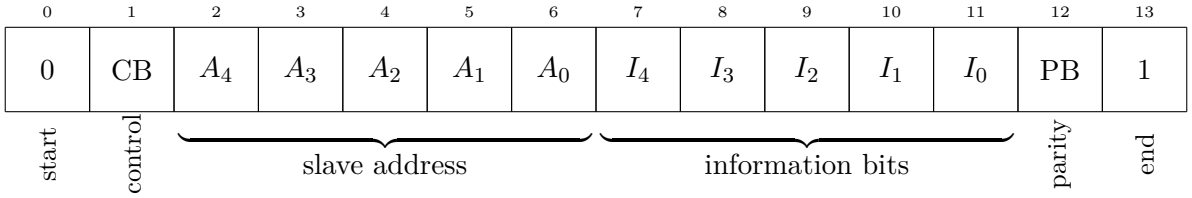


Figure 16.1: ASI packet format, master call

A) Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 16.2 and Manchester as per IEEE 802.3

3

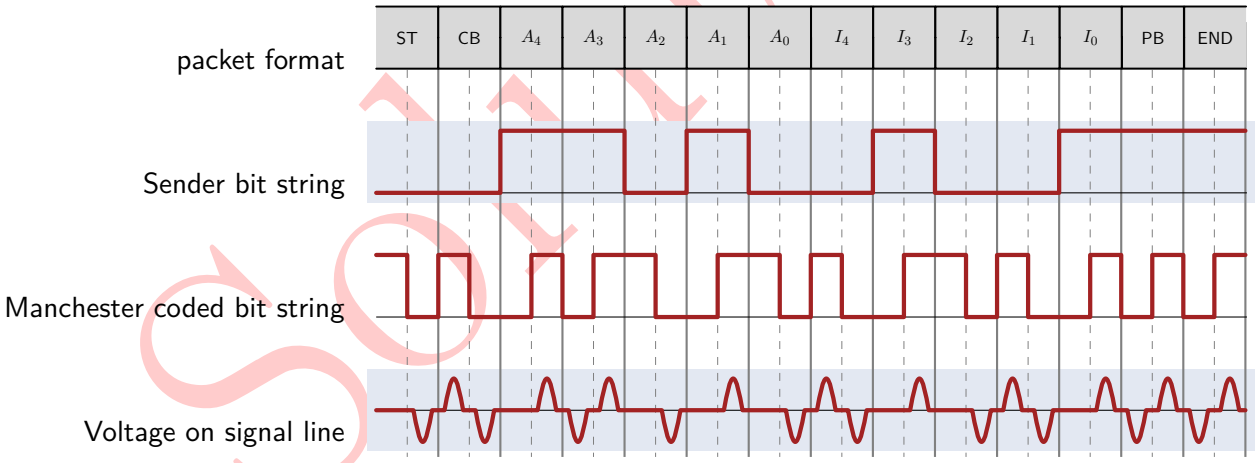


Figure 16.2: Waveform of the sender voltage

B) Figure 16.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

3

1. Start and stop bits: first impulse has to be negative, last impulse has to be positive
2. Succeeding impulses must have different polarity
3. Between two impulses of a telegram the pause that is allowed lasts half a bit time at maximum
4. The parity of the telegram must be even. In the example this cannot be seen since the transmitted data cannot be reconstructed due to the great amount of errors

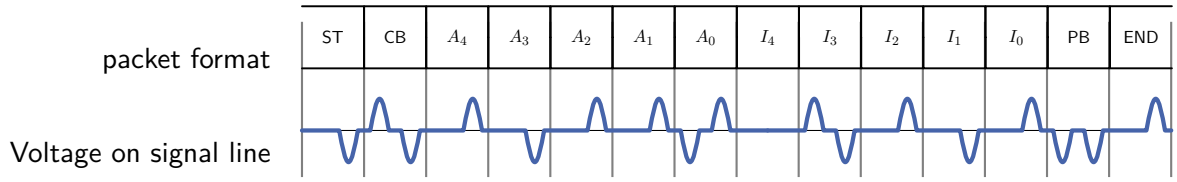


Figure 16.3: Waveform of the sender voltage

4

Task 17: CAN Bus

Since CAN uses CSMA/CA as arbitration scheme every participant compares the actual bus level with the signal transmitted by itself. Because of that it is important for every participant to be able to evaluate the actual state on the bus before begin of a new bit. Here beside the signal runtime on the bus also the required processing time of the participant itself plays a role.

As given in Figure 17.1, this includes the processing time t_{CAN} of the CAN controller, the times t_{Rx} and t_{Tx} which are needed inside the transceiver for reception and transmission as well as the runtime t_{Bus} on the bus.

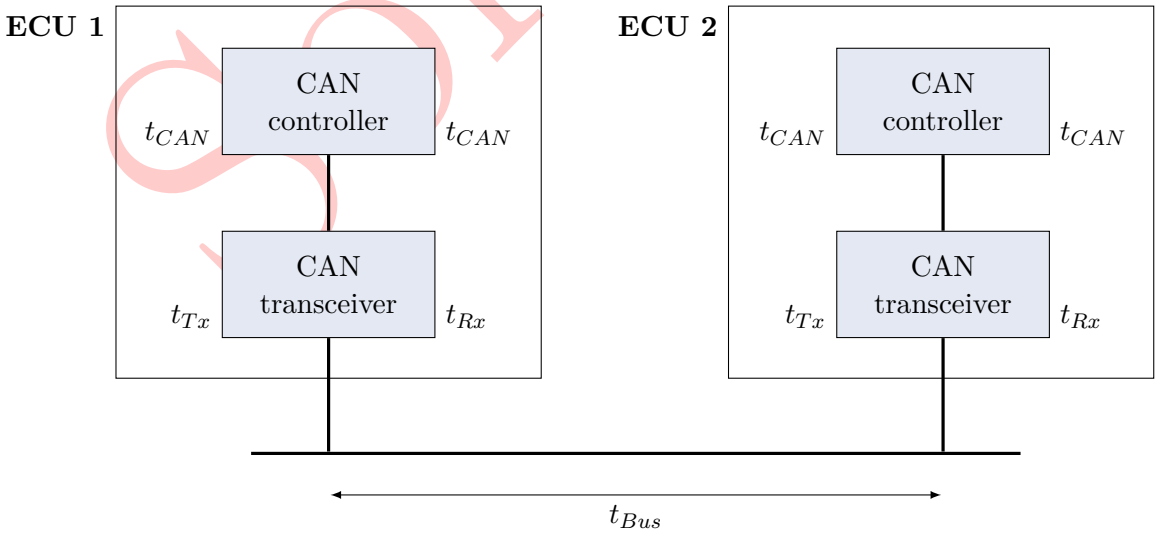


Figure 17.1: CAN bus

A) What is the interrelation between the maximum bus length and the bit transmission rate for CAN? Neglect the processing time inside the ECUs for this question

1

Condition of simultaneity has to be fulfilled.
T_{Bit}: Duration for transmission of one bit
T_{Prop}: Signal runtime on the bus

Interrelation: $T_{Bit} >> T_{Prop}$

$\Rightarrow \frac{1}{TR} >> \frac{l}{v}$
TRTransmission rate, l Maximum bus length, v Velocity of propagation

B) Based on the previous question, specify the maximum bus length for a speed of propagation of $v = 2.3 \cdot 10^8 m/s$ and for the transmission rates of $10 kbit/s$ and $1 Mbit/s$ respectively.

1

First node to start an arbitration has to wait at least 2 times the duration for propagation of a signal on the bus until it gets a valid signal on the bus:

- One node starts arbitration. After 1x T_{Prop} the signal reaches the node at the end of the bus.
- Now this node knows that a new arbitration has started and sends out its own ID bit.
- The signals reaches the first node after another T_{Prop}. Now we have a stable value on the bus, 2x T_{Prop} after the first node started transmission.

$T_{Bit} \geq 2 \cdot T_{Prop} \Rightarrow l \leq \frac{v}{2 \cdot TR}$
For $10 kbits/s$: $l \leq \frac{2.3 \cdot 10^8 m/s}{2 \cdot 10 kbit/s} \Rightarrow l \leq 11500m$
For $1 Mbit/s$: $\Rightarrow l \leq 115m$

C) Now also consider the delays inside the ECUs. Which data transmission rate can be set as a maximum if the bus length between the two controllers that have furthest distance amounts to 300 meters? The detection of the bus state shall be accomplished after 80 percent of the bit time at latest (assume: $t_{CAN} = 75nsec$, $t_{Rx} = t_{Tx} = 25nsec$, $v_{Bus} = 0,2m/nsec$).

2

Maximum transmission rate

Delay inside the participants:
$t_{TN} = 2 \cdot t_{CAN} + t_{Tx} + t_{Rx} = 2 \cdot 75ns + 2 \cdot 25ns = 200ns$
Delay on the bus:
$t_{Bus} = \frac{l_{Bus}}{v_{Bus}} = \frac{300m}{0.2m/ns} = 1500ns = 1.5\mu s$
Minimum bit duration:
$t_{Bit} \geq 2 \cdot (t_{TN} + t_{Bus}) = 2(0.2\mu s + 1.5\mu s) = 3.4\mu s$
Maximum transmission speed:
$S = \frac{0.8}{t_{Bit}} = \frac{0.8}{3.4\mu s} = 235 Kbit/s$

8

Task 18: PCI bus circle

Figure 18.1 shows the process of reading four data words within a burst on the PCI bus. The signals marked with "*" use negative logic. The FRAME* signal indicates the beginning and the end of a burst transaction. AD is the time multiplexed address- and data-bus. IRDY* (master) und TRDY* (slave) are used to insert waiting cycles after the transmission of an address. A waiting cycle is always inserted when at least one of the two signals is deactivated, that means it shows a high voltage level. All bus participants evaluate the state of a signal line at the rising edge of the clock. The clock frequency is 33.33MHz.

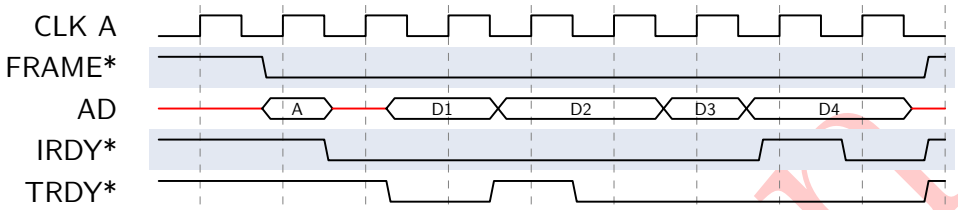


Figure 18.1: Simple PCI burst

A) How many waiting cycles are generated during the read burst given in Figure 18.1? 3

Criteria for a waiting cycle: After the address phase at least one of the signals IRDY* or TRDY* is HIGH.

- Cycle 2: IRDY* and TRDY* both are HIGH. Within this cycle the address is transmitted, so it is not a waiting cycle
- Cycle 3: TRDY* is HIGH → the target initiated the waiting cycle
- Cycle 5: TRDY* is HIGH → the target initiated the waiting cycle
- Cycle 8: IRDY* is HIGH → the initiator caused the waiting cycle

In total three waiting cycles are generated.

B) How long is the latency from the point in time when the activation of the FRAME* signal is detected by all bus participants to the point when the first data word can be read? 2

The FRAME* is recognized at the rising edge of cycle 2. The first data word is transmitted with the rising edge of cycle 4 since only then the slave signals the acceptance of the data by TRDY* = LOW.
The latency time results to: $2 \cdot \frac{1}{33.33MHz} = 2 \cdot 30ns = 60ns$

C) Assume that the address phase of a burst of infinite length has just ended and none of the involved participants forces waiting cycles. What is the data transfer rate of the PCI bus in this ideal case? (Approximation: $1MB = 10^6 Bytes$)

2

Width of the PCI bus: 32bit $\rightarrow$ 4 bytes per cycle
Duration of a cycle: $\frac{1}{33.33MHz} = 30ns$
Data transfer rate: $\frac{4Bytes}{30ns} = 133.33MBytes/s$

D) The time behavior of the PCI bus that can be seen in the picture is characteristic for a certain category of busses. What is the name of this category?

1

All signals are evaluated depending on the edge of a common clock signal $\rightarrow$ synchronous bus.

10

Task 19: Dijkstra

In Figure 19.1 you can see a network of six nodes (A..F). The nodes each have a different number of ports, numbered from #1 to #4. Each connection between the tiles is annotated with the communication cost. Your task is to generate the routing tables for the individual nodes.

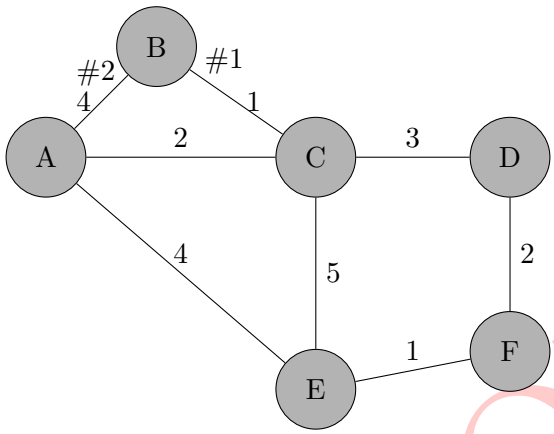


Figure 19.1: Given network topology

A) Determine the shortest path from node B to all other nodes using the Dijkstra-Algorithm. Make use of the tables 19.1 and 19.2. 5

B) Use the results from the previous task to generate the routing table of node B. 5

node	step 1 **B**		step 2		step 3		step 4		step 5	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A	∞	-	4	B	3	C	3	C	3	C
B	∞	B	0	B	0	B	0	B	0	B
C	∞	-	1	B	1	B	1	B	1	B
D	∞	-	∞	-	4	C	4	C	4	C
E	∞	-	∞	-	6	C	6	C	6	C
F	∞	-	∞	-	∞	-	∞	-	6	D

Table 19.1: Dijkstra algorithm

node	step 6		step 7	
vertex	dist.	pred.	dist.	pred.
A	3	C	3	C
B	0	B	0	B
C	1	B	1	B
D	4	C	4	C
E	6	C	6	C
F	6	D	6	D

Table 19.2: Dijkstra algorithm

7

Task 20: Serial Interface

In the figure 20.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit (‘0’), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as 1 or 2 stop bits (‚1’). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

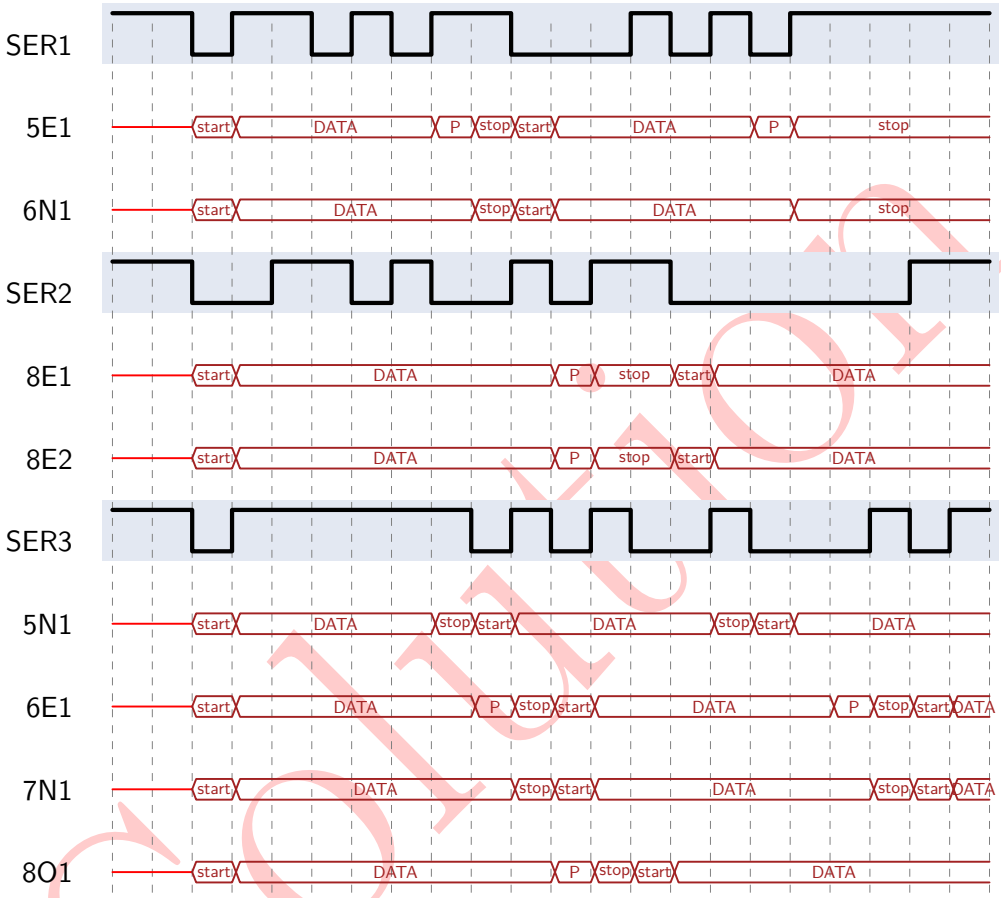


Figure 20.1: Serial interface pulse diagram

A) Give all possible frame formats for the pulse sequences as shown in figure 20.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep. 4

B) In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams. 2

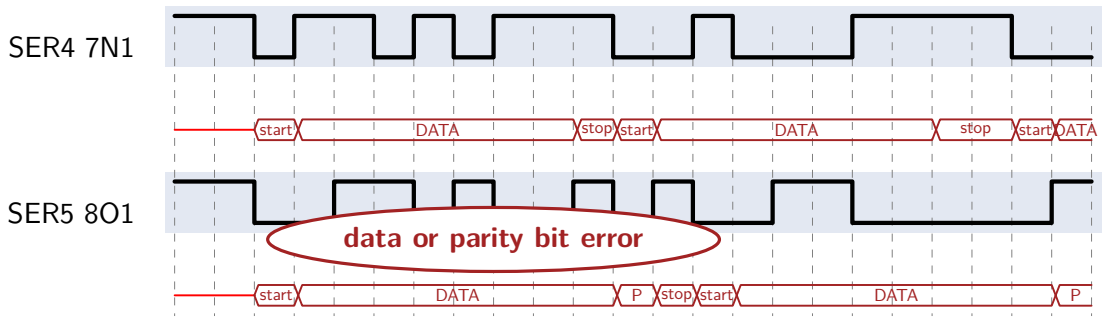


Figure 20.2: RS232 pulse sequences

C) Is it possible to detect errors without knowing the frame formats? **1**

c) Not in general. The frame format gives the position and meaning of a parity bit for example.

16

Task 21: Networks

Task 21.1: General Questions

A) Name three basic building blocks in a Network-on-Chip and explain their function. **2**

Network Interface: Mediating between Computing Unit and Network
Routing Unit: Embedded intelligence that decides on the direction of the data
Link : Physical communication channel between neighboring nodes.

B) Which type of switching is preferable in a NoC where the computing units mainly communicate by streaming data, thus in need of high and guaranteed throughput. Justify your decision. **1**

Circuit Switching, easier to guarantee throughput

C) What is the edge connectivity and diameter of a 4x4 Torus ? **2**

4,4

Task 21.2: Routing

Figure 21.1 shows a 4x4 Mesh network with packet-switching communication.

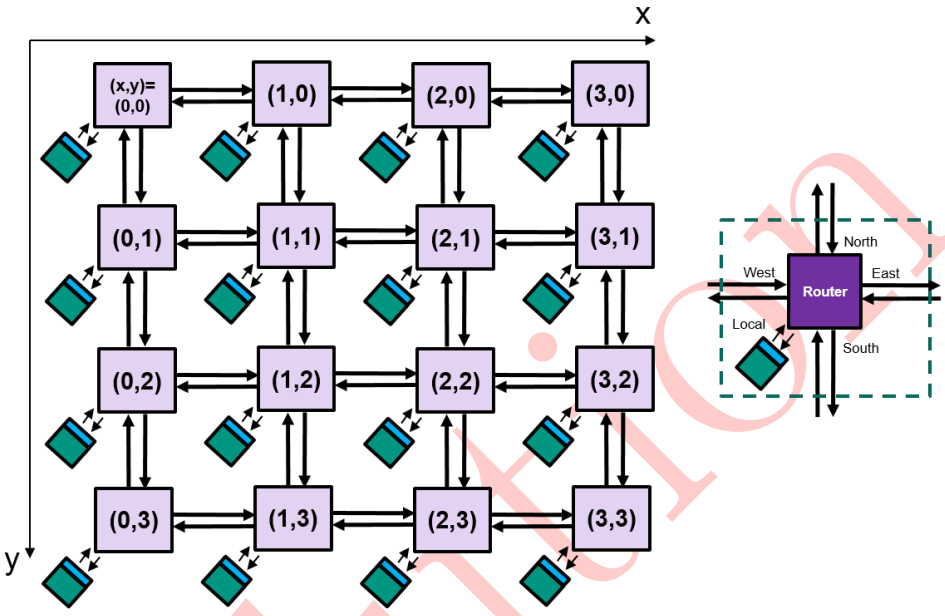


Figure 21.1: 4x4 Mesh network

A) Name all the traversed routers when a packet is sent from $(x, y) = (1, 0)$ to $(3, 3)$ using common XY-Routing. Please provide the coordinates of the traversed router.

1

$(1, 0)$, $(2, 0)$, $(3, 0)$, $(3, 1)$, $(3, 2)$, $(3, 3)$

B) The routers at address $(1, 0)$ and $(2, 1)$ are experiencing heavy traffic at their east port, such that packets have to wait before being forwarded. To handle such cases a custom routing algorithm called as the "XY-YX" was designed. The "XY-YX" algorithm is described as follows: When a packet arrives, an output port is chosen using the XY routing. If the output port is not busy, the packet is forwarded. If the output port chosen is busy, YX routing is applied to the packet and a new output port is computed. Name all traversed nodes when a packet travels from $(x, y) = (1, 0)$ to $(3, 3)$?

2

$(1,0)$, $(1,1)$, $(2,1)$, $(2,2)$, $(3,2)$, $(3,3)$

C) Which categories of routing algorithms is the "XY-YX" routing described above associated with? Explain your answer. **2**

Adaptive Routing: Since Ports are used depending on Traffic in Routers
Distributed Routing : Routing computations is done in the nodes Minimal Routing: Packets travel using minimum number of hops

D) Now only the east port of router at (1,1) is busy in the network. Using the same "XY-YX" routing described before, name all traversed routers when the source is (0,1) and destination is (3,1). What do you notice ? **1**

Packet gets stuck at (1,1).
The Packet can get discarded because the algorithm does not store the packet.

E) An additional feature was added to the "XY-YX" algorithm. If the chosen output port is busy even after the YX algorithm was used by the router, then another output port is chosen among the remaining ports according to the priority : North > East > South > West. Now name all traversed routers when the source is (0,1) and destination is (3,1). Again only the east port of router at (1,1) is busy in the network. Is the new routing algorithm minimal ? **2**

$(0,1)$, $(1,1)$, $(1,0)$, $(2,0)$, $(3,0)$, $(3,1)$
No. The packets travel away from the destination. They choose non-minimal path as seen in this case.

F) Now the busy ports are at the south and east of router at (1,1). There is another busy port at south of router (2,0). Use the "XY-YX" routing algorithm with the additional feature mentioned in the above task. Now name all traversed routers when the source is (0,1) and destination is (2,2). What do you notice ? **2**

(0,1) -> (1,1) -> (1,0) -> (2,0) -> (3,0) -> (2,0)
We see a livelock

G) Describe two scenarios: one in which XY Routing is preferable and one in which the "XY-YX" routing is preferable. **1**

Balanced network traffic XY Routing will find the shortest Path
If heavy traffic is present at certain ports, "XY-YX" routing can reduce the latency

9

Task 22: Quadrature Amplitude Modulation

A) What is the difference between the PSK and the QAM modulation technique? 1

PSK modulates only the signal phase while QAM additionally modulates the amplitude of the signal. **+1P for correct answer**

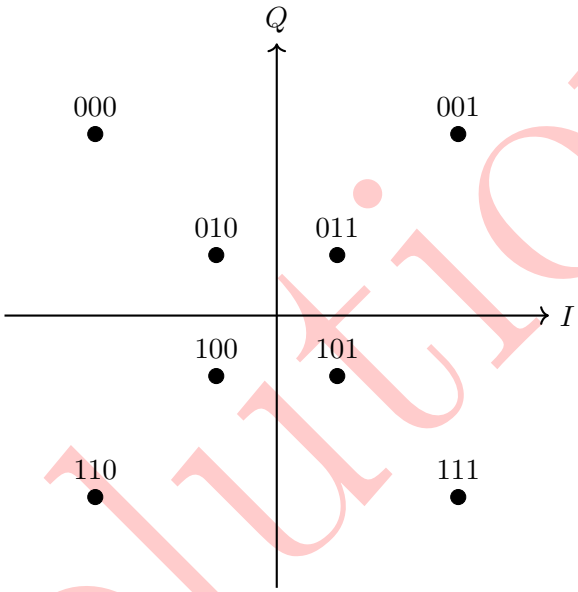


Figure 22.1: Constellation diagram

B) Figure 22.1 shows a constellation diagram for a digital modulation technique. Which type of modulation is used here? Which properties of the signal can be varied with this modulation type? 1

Modulation type: 8-QAM
Varied properties: Phase and Amplitude

+0.5P for 8-QAM
+0.5P for correct properties

C) The symbol constellation from Figure 22.1 is now used by a transmitter to modulate data bits on a carrier. The phase φ of the signal is defined relative to a sine reference signal as shown in Figure 22.2. A receiver device now picks up the modulated signal which is plotted in Figure 22.3. Which bits have been transmitted by the sender? Demodulate the signal and write down the resulting bit-stream.

3

Transmitted bits:
($\varphi = -\frac{\pi}{4}$, HIGH amplitude)111
($\varphi = -3\frac{\pi}{4}$, LOW amplitude)100
($\varphi = -\frac{\pi}{4}$, LOW amplitude)101
($\varphi = \frac{\pi}{4}$, HIGH amplitude)001

+3P for correct solution
-1P per incorrect symbol

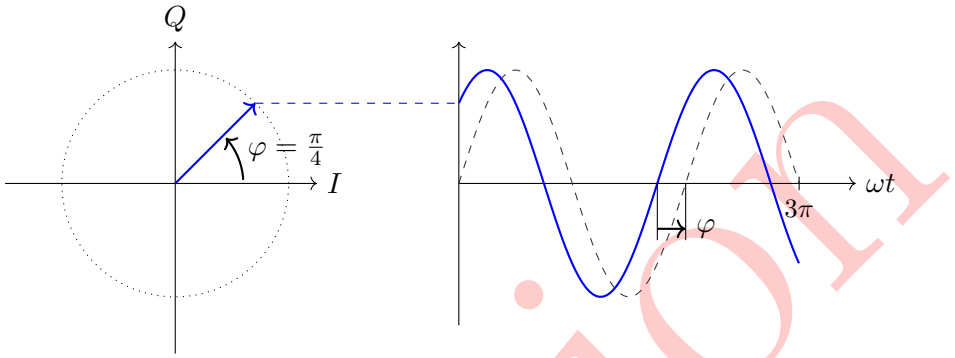


Figure 22.2: Phase difference of a sine signal compared to a reference signal (dashed line $\widehat{=}$ reference signal).

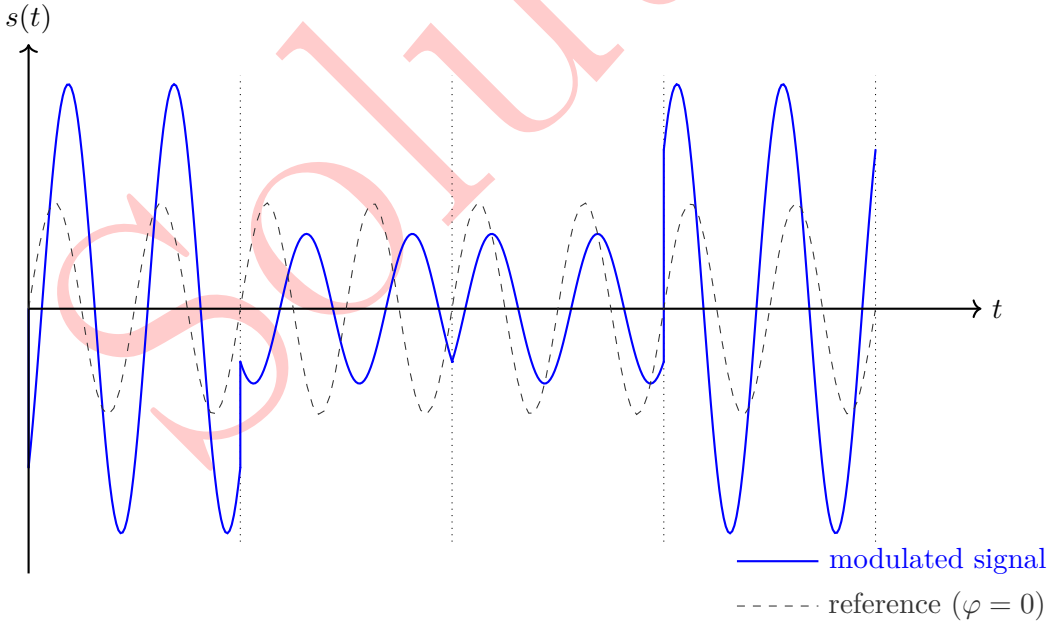


Figure 22.3: A modulated signal which uses the constellation from Figure 22.1 on the preceding page.

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D) Now, a signal is modulated with the constellation diagram from Figure 22.4 and transmitted on a coaxial cable. The sender is able to generate a maximum voltage amplitude U_{max} of $\pm\sqrt{72}\,V$. Calculate the acceptance radius r_a for the symbols in the constellation diagram.

3

From the constellation diagram geometry: $(2 \cdot U_{max})^2 = (3\,(2r_a))^2 + (3\,(2r_a))^2$

+1P for correct approach

$(2 \cdot U_{max})^2 = 72\,r_a^2$

+1P for equation solving

$r_a^2 = \frac{(2U_{max})^2}{72}$

+1P for calculating the solution

$r_a = \sqrt{\frac{(2U_{max})^2}{72}}$

Insert numbers: $r_a = \sqrt{\frac{4 \cdot 72}{72}}\,V \;=\; \sqrt{4}\,V \;=\; 2\,V$

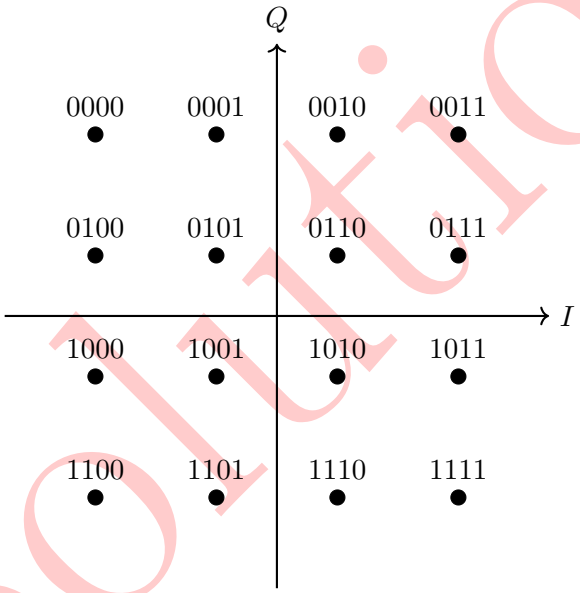


Figure 22.4: Constellation diagram

E) The symbol acceptance radius is a deciding factor for the symbol error probability. However the bit error probability also depends on the encoding of the symbols. The symbol-encoding in Figure 22.4 is not optimal because multiple bits can flip when neighboring symbols are mixed-up due to signal noise. Which kind of encoding could help to solve this problem?

1

Gray-codes with a Hamming distance of 1 between neighboring symbols would solve this problem.

+1P for usage of gray-codes

4

Task 23: Signal Classes

4

A) The signal in Figure 23.1 is given as the original analog signal. Transform this signal into the other signal classes. Describe for each of the classes how the sampled signal is generated. Use the diagrams in Figure 23.1 to 23.3 with the given sampling points.

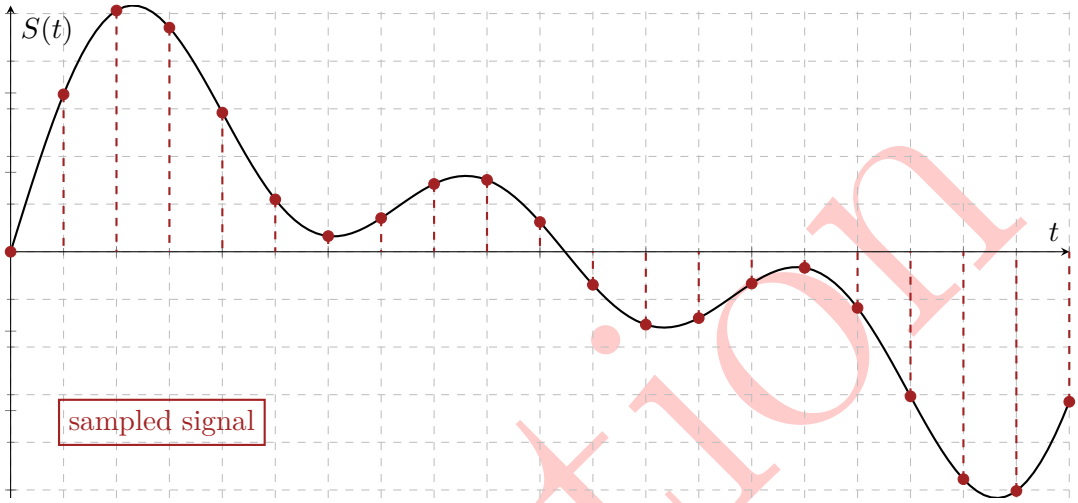


Figure 23.1: signal class:

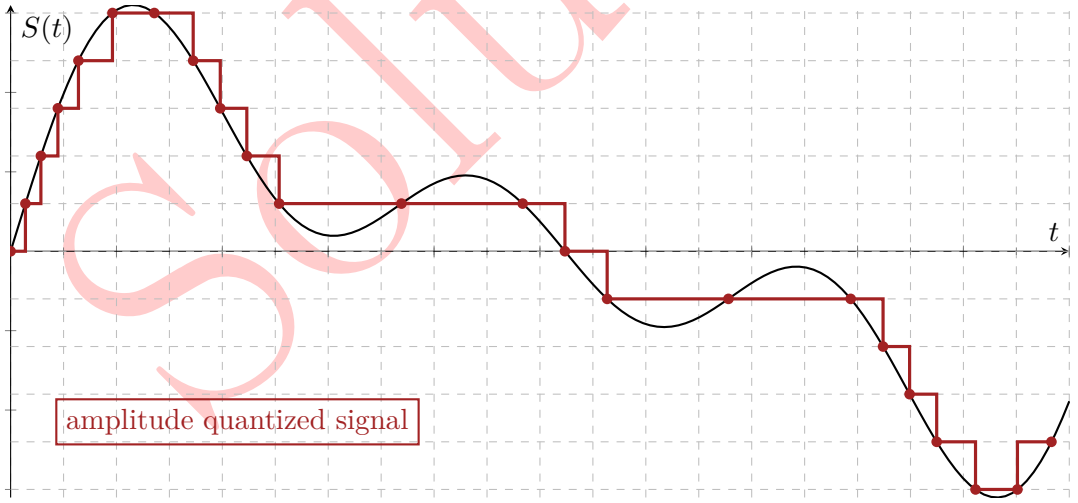


Figure 23.2: signal class:

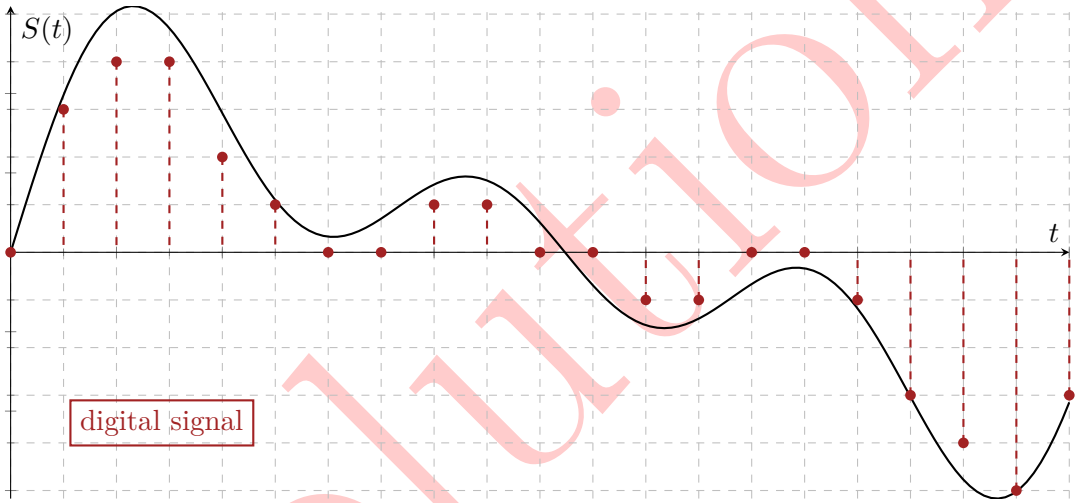


Figure 23.3: signal class:

6

Task 24: Flow Control

A communication system is given in Figure 24.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a Level-triggered Closed-loop Flow Control protocol corresponding to Figure 3.1 for the high-level synchronization.

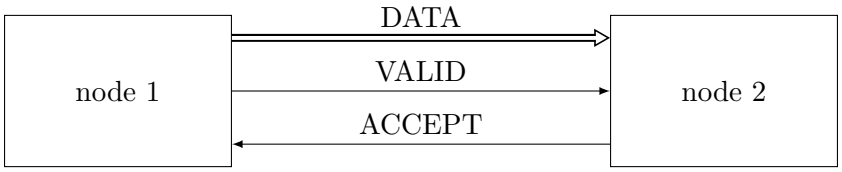


Figure 24.1: Communication system applying Level-triggered Closed-loop Flow Control procedure

A) In Figure 24.2 the sensitive clock edges of the sender and the receiver as well as the signal values for the first sender clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the valid signal is set to '1' by the sender. The receiver will also set the accept signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

4

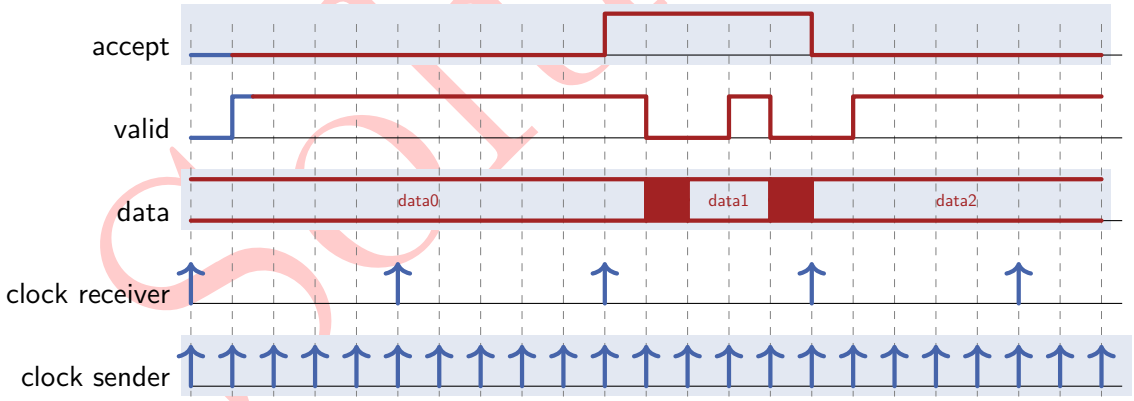


Figure 24.2: Signal progression diagram

B) Is this kind of synchronization free from error in this specific case? Justify your answer.

1

No. One can see that data1 got lost because it was put on to the data lines and removed by sender while receiver is still busy processing data0.

Recognize that data1 is lost +0.5P
Correct reasoning for the data lost +0.5P

C) Propose a better solution for this communication scenario.

1

1. Clock divider in sender so that both are only clocked at 200 kHz
2. Edge-triggered Closed-loop Flow Control
3. Clock down the sender: to avoid this loss of data, the following equation must be satisfied: $3T_r \leq 2T_r + 4T_s \Rightarrow T_r \leq 4T_s$

Recognize that data1 is lost +0.5P
Correct reasoning for the data lost +0.5P

2

Task 25: Universal Serial Bus (USB)

A) Consider an USB 1.1 device in reset state. Calculate the current on the bus. Neglect the energy needs of the device itself. Use the circuit in Figure 25.1 as orientation. 1

The current flow on the bus is determined by the series connection of R_1 and R_2:

$$R_1 + R_2 = 15k\Omega + 1,5k\Omega = 16.5k\Omega$$

$$I = \frac{U}{R} = \frac{3.3V}{16.5k\Omega} = 200\mu A$$

As a comparison: Maximum current consumption in standby in accordance with the specification: $500\mu A$.

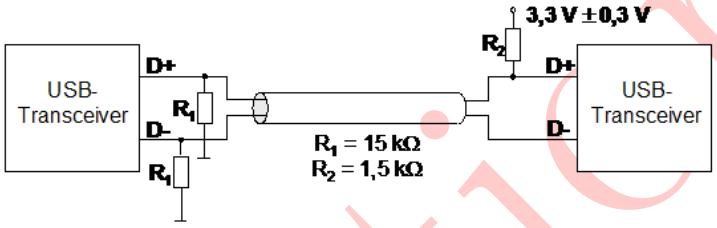
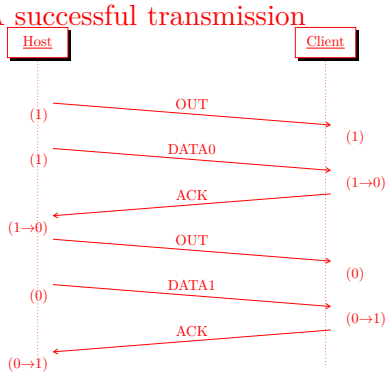


Figure 25.1: Example for resistor configuration at 12Mbit/s

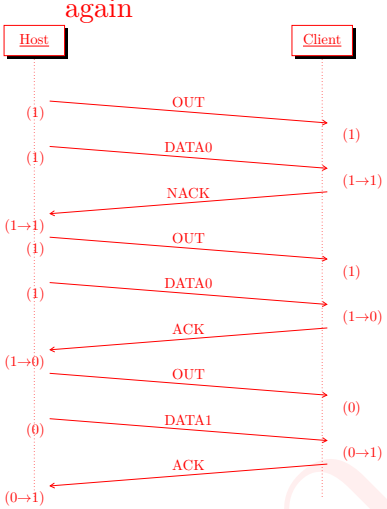
B) To reduce the probability of errors during the handshake phase of a transaction, two data PIDs (DATA0 and DATA1) are used. The data PID is changed after every successful transmission. For that reason the sender and the receiver both have a „data toggle sequence bit“. At the receiver this only changes if correct data with a correct PID has been accepted. At the sender it changes when a valid ACK-Handshake is received. Both participants of a transmission first have to synchronize their bits during the setup phase of a control transfer (see Figure 25.2, the bracketed values correspond to the value of the “data toggle sequence bits”; at X/Y they are still undefined). 1
Starting from the state of 25.2, specify the flow charts for the following cases (always consider a transfer from host to device):

1. A successful transmission
2. A data packet is rejected and only accepted after being transmitted again
3. The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then

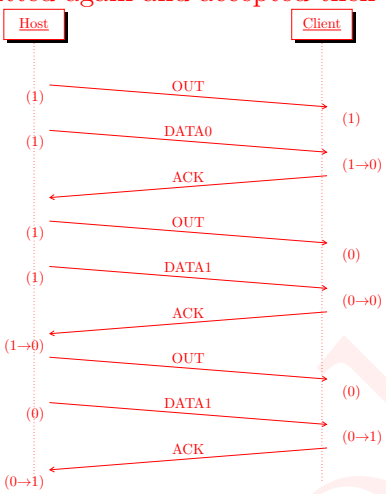
A successful transmission



A data packet is rejected and only accepted after being transmitted again



The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then



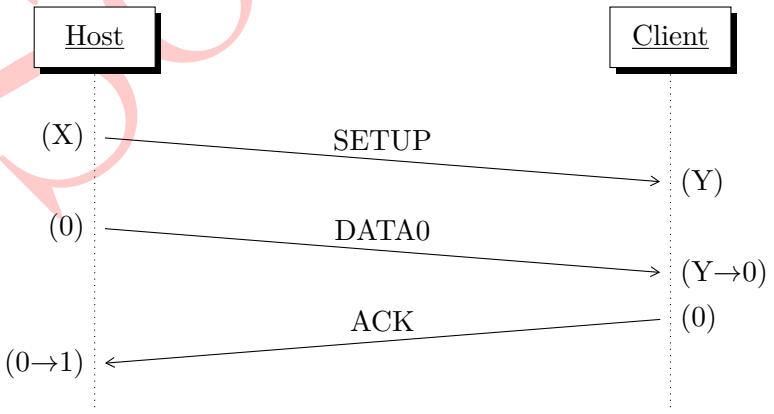


Figure 25.2: Synchronization of the data toggle sequence bits

7

Task 26: Flexray: Bus Access

In this task we want to investigate the data transmission and scheduling with Flexray. The used topology is shown in Figure 26.1. Additionally, the slot durations for the scheduling are given in Table 26.1.

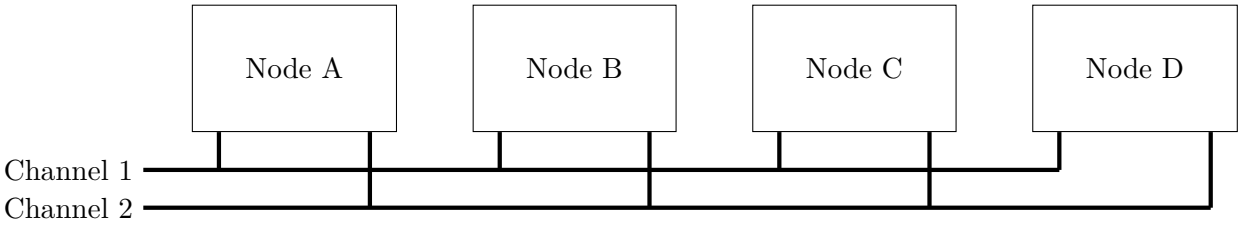


Figure 26.1: Flexray Topology

Static slots	Minislots
$5\mu s$	$100ns$

Table 26.1: Slot durations

A) In Table 26.2 the nodes shown in Figure 26.1 and the assignment of their available frames to the static slots are given. Complete the signal diagram in the Figure 26.2 and perform the static scheduling of the frames according to the Table 26.2. 2

Node	Static Slots	Frames	Redundant Frames
A	1, 3, 5	A1, A2, A3	A2
B	2, 4	B1, B2	B2
C	1, 4	C1, C2	—
D	5	D1	—

Table 26.2: Static Node Assignments

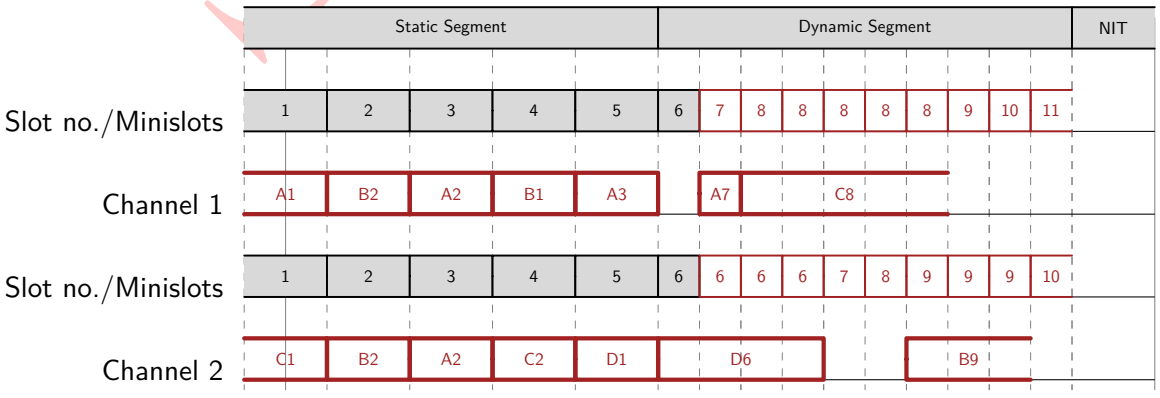


Figure 26.2: Signal sequence

B) Calculate the duration of a complete communication cycle! Assume a Network Idle Time (NIT) of $1\mu s$ and that all minislots depicted in Figure 26.2 are idle! **1**

$5 * t_{static} + 10 * t_{dynamic} + t_{NIT} = 5 * 5\mu s + 10 * 0.1\mu s + 1\mu s = 27\mu s$

C) What is the purpose of the minislots with regard to bus access, which are used in the dynamic segment of the communication cycle? Is it possible that multiple nodes can own the same minislot? Justify your answer! **2**

Prioritized bus access within the dynamic segment controlled with a slot count. Not possible for multiple nodes to own the same minislot: Similar to static slots each minislot is exclusively owned by one FlexRay node. A minislot thereby only defines a potential start time of a frame transmission in the dynamic segment.

+1 pt. for each question.

D) In Table 26.3 the parameters for the dynamic segment are given. Complete the signal diagram in the Figure 26.2 and perform the dynamic scheduling of the frames for Channel 1 and Channel 2 according to the Table 26.3. Number the minislots with slot IDs dependent on the length of your scheduled frames. Note that each channel offer its own minislots for transmission. **2**

Node	Frames	Slot-ID	Frame Duration
A	A7	7	$100ns$
B	B9	9	$300ns$
C	C8	8	$500ns$
D	D6	6	$400ns$
	D11	11	$200ns$

Table 26.3: Dynamic Segment Parameters